REMARKS

The rejections and comments of the Examiner set forth in the Office Action dated March 29, 2001 have been carefully reviewed by the Applicants. Additionally, informalities in the specification have been corrected. No new matter has been added.

The disclosure has been objected due to a reference to "clock buffer 524" on page 22, line 8 that is not found in Figure 5B. The reference to "clock buffer 524" has been changed to "clock buffer 526", and the reference character string "525" in Figure 5B has been changed to "526". In both the drawings and the disclosure, the reference character string "524" has been used to refer to a "lock-up" latch, and the reference character string "525" has been used to refer to a "select line input". The description of the "clock buffer" clearly applies to the drawing element in Figure 5B that was previously referenced as "525". The Applicants respectfully submit that the amendment of "clock buffer 524" in the specification and the amendment of element "525" in Figure 5B are made as corrections of obvious errors, and as such, do not constitute new matter.

Claims 22-26 are currently rejected under 35 U.S.C. 112, second paragraph, as being indefinite to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 22,24,25 and 26 have been amended so as to provide the requisite antecedent basis per M.P.E.P. 2173.05(e). Claim 22 has been amended to provide antecedent basis for "the clock domain". Claim 24 has been amended to provide antecedent basis for "the relative positions". Claim 25 has been amended to provide antecedent basis for "the respective surrounding cone logic".

Claim 26 has been amended to provide antecedent basis for "the respective switching times".

Claims 1-26 are currently rejected under 35 U.S.C 102(a) as unpatentable over Beausang et al. (U.S. Patent No. 5703,789) in view of Crouch et al. (U.S. Patent No. 5,592,493). The Applicants respectfully traverse the rejection on the grounds that Crouch et al is directed method involving "clock cycle" domains and does not address "clock" domains as disclosed in the present invention. In examining Crouch et al. in its entirety, it can be seen that all references to "clock cycle" domains and "clock" domains are restricted to references found in the paragraph beginning at col 12 line 52:

FIG. 14 shows this process in detail. A single concatenated scan chain (such as the present example of testing block 32) consists of all scan elements connected from the STDI pin to the STDO pin. A subset of this architecture is shown here connected between SDI and SDO. The path 312 comprised of nets, nodes, gates, transistors, and other logic devices is a path within a grouping of logic 302 and has been identified as a critical path which must meet the condition that the sampled response E in scannable element 310 arrive at one fixed clock edge from its launch from scannable element P (e.g., a logic 1 to logic 0 transition must occur at E within a time period of 20 nano-seconds, for a 50 MHz clock rating, after the proper launch value, for example a logic 0 to logic 1 transition at point P). In order for the transition that occurs at E to be directly a result of the change in value at P, the path itself must be conditioned to pass the transition. This is done by fixing the off-path values (e.g., the other inputs to an AND gate other than the one input directly in the path) by tracing back through the logic and placing the correct value in scannable elements (as shown by the logic value 1 cells in scan chain segment 306). It can be seen that in order for the transition to occur at E, a transition must occur at P and all of the path establishing values must also occur, but in the previous clock cycle domain to the expected transition. In order to achieve the transition at P, logic one clock cycle domain earlier than this must be established (noted as 2 for 2nd clock domain in scan chain segment 304). This is why two sample cycles occur (see FIG. 12). An initial vector is scan shifted into the scan chain which establishes the logic values noted as 2 in scan chain segment 304 and also establishes the fixed values noted as 1 and P in scan chain segment 306. The applied values noted as the numeral 2 propagate through the logic grouping 300 and place pre-determined logic values on the D pins of the scannable elements marked as P and 1 in scan chain segment 306. The element 322 may be a logic value the propagates through a path 320 and applies a logic value to element 318 in scan chain section 306 that would cause it to hold

its value the same. The logic values in scan elements 328 and 330 may propagate through paths noted as 324 and 326 to cause the value of P to transition. When the first sample cycle is done (i.e., a rising-edge of PCLK is done), the scannable elements noted as 1 in scan chain section 306 will update causing the values noted as 1 to remain the same while a transition occurs on P. The values that are now in scan chain section 306 will cause the off-path values of path 312 to remain the same while the transition that just occurred at P will propagate through to the D input of element 310. On the next rising edge of PCLK, the element 310 should capture the transition noted as E.

As used by Crouch et al., the term "clock cycle domain" refers to a period of time and defines a temporal quantity. This is reinforced in the above paragraph by the use of the adjective "previous" to modify the term "clock cycle domain" at col 13 line 8 and the use of the phrase "...one clock cycle domain earlier..." at col 13 line 10. The only usage of the term "clock domain" at col 13 line 11 is actually a reference to a "clock cycle domain" as can be seen from the context.

In contrast, the term "clock domain" as used in the present invention and in the art in general refers to a spatial domain, more specifically, a "clock domain" is a region of a circuit in which the timing behavior is identical or very similar. Clock domain boundaries can be established on the basis of multiple clocks driving different parts of a circuit, or can be set by the presence of buffers, DLLs or PLLs.

Since the "clock domain" in the present invention as claimed is fundamentally different from the "clock cycle domain" or "clock domain" of Crouch et al., the Applicants respectfully submits that the present claimed invention is patentable over the combination of Beausang et al. and Crouch et al. In summary, Applicants assert that Claims 1-26 are now in condition for allowance and earnestly solicits such action by the Examiner.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

1. The second paragraph on page 22 beginning with It is also desirable..." has been replaced with the following paragraph:

Figure 5B is a logical block diagram illustrating another scan chain segment 515 on which the present invention can be applied. As illustrated, the scan chain segment 515 includes scan cells 520p-520t which consist of multiplexed D input flip-flops linked together to form a shift register configuration. Also illustrated is clock buffer 52[4]6 which is inserted on the clock signal line 531 between cells 520s and 520t.

2. The second paragraph on page 26 beginning with It is also desirable..." has been replaced with the following paragraph:

It is also desirable to place simultaneously switching cells on different power rails because the maximum amount of switching that happens in a design is typically during scan. Such requirements could limit the size of the partitions identified for re-ordering. Accordingly, at step 660, subsets 655 are individually partitioned according to simultaneously switching output (SSO) requirements of scan cells of the pertinent set. As illustrated, one subset 655b is partitioned into final sets 665a-665n at step_660. Data representative of the final sets 665a-665n is then provided to layout process 350 as partitioning information of the scan chain 605.

3. The second paragraph on page 27 beginning with "It should be appreciated that..." has been replaced with the following paragraph:

It should be appreciated that the order in which steps 610, 620, 630, 640, 650, and 660 of Figure 6 are performed is immaterial. Rather, the aforementioned steps may be performed in an arbitrary order. For instance, scan chain partitioning step 660 based on SSO requirements may be performed prior to partitioning step 650. Furthermore, one or more of steps 610, 620, 630, 640, 650, and 660 may be omitted. Any permutations, combinations or variations of the above order should be construed to be different embodiments within the scope of the present invention. Table 1 below illustrates some ex[a]emplary variations of the partitioning order in furtherance of the present invention.

IN THE CLAIMS

Claim 22 has been amended as follows:

22. (Amended) A method of constructing a scan chain comprising the steps of:

a) adding scan cells to a netlist description of an integrated circuit design having a plurality of clock domains, said scan cells being coupled serially together to form a first scan chain having a scan cell ordering;

b) partitioning said scan cells of said first scan chain into sets of scan cells and generating partitioning information indicative thereof, said step b) comprising the steps of:

b1) partitioning said scan cells of said first scan chain into sets according to the clock domain of said scan cells wherein scan cells of a given set share the same clock domain; and

b2) partitioning scan cells of said sets of step b1) into subsets according to edge sensitivity of said scan cells wherein scan cells of a given subset share the same edge sensitivity and the same clock domain; and

c) constructing a second scan chain by breaking said scan cell ordering of said first scan chain and reordering said scan cells based on said partitioning information wherein only scan cells of a same set are allowed to be reordered.

Claim 24 has been amended as follows:

24. (Amended) The method as described in Claim 23 wherein said first scan chain comprises a reconfigurable multiplexer positioned relative to the scan cells of said first scan chain and wherein said step b) further comprises the step of partitioning scan cells of said subsets of step b2) into subsets according to the relative positions of said scan cells to [a] the reconfigurable multiplexer of said first scan chain wherein scan cells of a given subset share the same edge sensitivity, the same clock domain and the same relative position to said reconfigurable multiplexer.

Claim 25 has been amended as follows:

25. (Amended) The method as described in Claim 23 wherein said first scan chain and said second scan chain each comprise a surrounding cone of logic and

wherein said step b) further comprises the step of partitioning scan cells of said subsets of step b2) into subsets according to the respective surrounding cone logic of [said] the scan chains wherein scan cells of a given subset share the same edge sensitivity, the same clock domain and the same surrounding cone logic.

Claim 26 has been amended as follows:

26. (Amended) The method as described in Claim 23 wherein each of said first scan chain and said second scan chain comprise a switching time and wherein said step b) further comprises the step of partitioning scan cells of said subsets of step b2) into subsets according to the respective switching times of [said] the scan chains wherein scan cells of a given subset share the same edge sensitivity, the same clock domain and the same power rail.